iC-HG

3 A LASER SWITCH

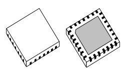
FEATURES

- Six channel laser switch from CW up to 200 MHz
- CW operation with up to 500 mA per channel
- Spike-free switching of the laser current
- 6 x 1 channels with TTL inputs
- 3 x 2 channels with LVDS inputs
- Operates as six independent voltage-controlled current sinks
- Switching outputs (LDKx) are 12 V capable for blue laser diodes
- Fast and slow switching mode
- Simple current control at pins CIx
- CIx voltage < 3 V for full current
- Wide supply voltage range from 3 to 5.5 V
- All channels can be paralleled for 3 A operation
- Multiple iC-HG can be connected in parallel for higher currents
- Open drain error output
- Thermal shutdown

APPLICATIONS

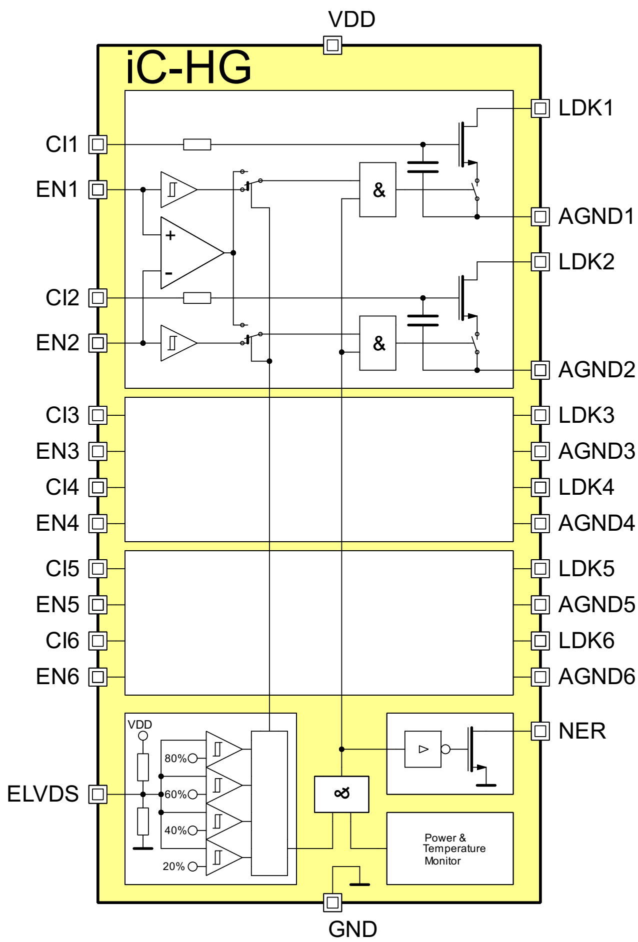
- Pump lasers
- Laser projection
- Laser TV

PACKAGES



QFN28 5 mm x 5 mm

BLOCK DIAGRAM



DESCRIPTION

Six channel Laser Switch iC-HG enables the spike-free switching of laser diodes with well-defined current pulses at frequencies ranging from DC to 200 MHz.

The diode current is determined by the voltages at pins CIx.

The six fast switches are controlled independently via TTL inputs. Input ELVDS = hi selects LVDS type inputs and three channel mode. *TTL slow switch mode* is selected with 30% VDD and *LVDS slow switch mode* with 70% VDD at input ELVDS.

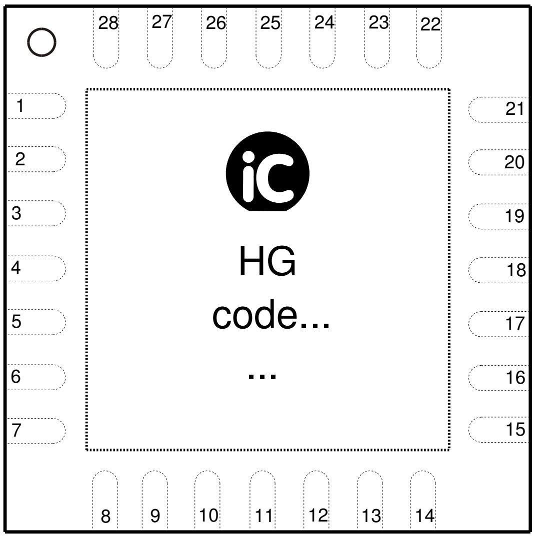
The laser diode can thus be turned on and off or switched between different current levels (LDKx connected) defined by the voltages at CIx.

Each channel can be operated up to 500 mA DC current depending on the heat dissipation.

The integrated thermal shutdown feature protects the iC-HG from damage by excessive temperature.

PACKAGES QFN28 5 mm x 5 mm to JEDEC

PIN CONFIGURATION QFN28 5 mm x 5 mm



PIN FUNCTIONS

No.	Name	Function
1	CI1	Current control voltage channel 1
2	CI2	Current control voltage channel 2
3	CI3	Current control voltage channel 3
4	GND	Ground
5	CI4	Current control voltage channel 4
6	CI5	Current control voltage channel 5
7	CI6	Current control voltage channel 6
8	AGND6	Analog ground channel 6
9	LDK6	Laser diode cathode channel 6
10	AGND5	Analog ground channel 5
11	LDK5	Laser diode cathode channel 5
12	AGND4	Analog ground channel 4
13	LDK4	Laser diode cathode channel 4
14	EN6	TTL switching input channel 6 Negative LVDS Input channel 5 and 6
15	EN5	TTL switching input channel 5 Positive LVDS Input channel 5 and 6
16	EN4	TTL switching input channel 4 Negative LVDS Input channel 3 and 4
17	EN3	TTL switching input channel 3 Positive LVDS Input channel 3 and 4
18	VDD	Supply voltage
19	ELVDS	TTL/LVDS Fast/Slow Input selector
20	EN2	TTL switching input channel 2 Negative LVDS Input channel 1 and 2
21	EN1	TTL switching input channel 1 Positive LVDS Input channel 1 and 2
22	NER	Error monitor output
23	LDK3	Laser diode cathode channel 3
24	AGND3	Analog ground channel 3
25	LDK2	Laser diode cathode channel 2
26	AGND2	Analog ground channel 2
27	LDK1	Laser diode cathode channel 1
28	AGND1	Analog ground channel 1

The *Thermal Pad* is to be connected to a *Ground Plane* (GND, AGND1. . . 6) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC HG label and coding is subject to change).

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.3	6	V
G002	I(VDD)	Current in VDD		-10	750	mA
G003	V(CI)	Voltage at CI1. . . 6		-0.3	6	V
G004	V()	Voltage at EN1. . . 6, AGND1. . . 6, ELVDS, NER		-0.3	6	V
G005	V(LDK)	Voltage at LDK1. . . 6		-0.3	12	V
G006	I(LDK)	Current in LDK1. . . 6	DC current	-10	600	mA
G007	I(AGND)	Current in AGND1. . . 6	DC current	-600	10	mA
G008	I()	Current in CI1. . . 6, EN1. . . 6, ELVDS		-10	10	mA
G009	I(NER)	Current in NER		-10	20	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Operating Junction Temperature		-40	125	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended range on request)		-25		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient			tbd		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0...5.5 V, AGND1. . . 6 = GND, Tj = -25...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device (x = 1. . . 6)							
001	VDD	Permissible Supply Voltage		3		5.5	V
002	I(VDD)	Supply Current in VDD	CW operation ELVDS = GND ELVDS = 30% VDD ELVDS = 70% VDD ELVDS = VDD			 tbd tbd tbd tbd	 mA mA mA mA
003	I(VDD)	Supply Current in VDD	pulsed operation, f(ENx) = 200 MHz			700	mA
004	V(LDKx)	Permissible Voltage at LDKx		-0.3		12	V
005	V(NER)	Permissible Voltage at NER		-0.3		5.5	V
006	Vc()hi	Clamp Voltage hi at LDKx	I(LDK) = 10 mA	12.1		18	V
007	Vc(NER)	Clamp Voltage hi at NER	I(NER) = 1 mA	7	15	18	V
008	Vc(CIx)hi	Clamp Voltage hi at CIx	Vc(CIx) = V(CIx) − VDD; I(CI) = 10 mA, other pins open	0.3		1.6	V
009	Vc()hi	Clamp Voltage hi at ENx, ELVDS	Vc() = V() − VDD; I() = 1 mA, other pins open	0.8		3	V
010	Vc()lo	Clamp Voltage lo at VDD, LDKx, CIx, ENx, AGNDx, ELVDS, NER	I() = -10 mA, other pins open	-1.6		-0.3	V
Laser Control LDK1. . . 6, CI1. . . 6 (x = 1. . . 6)							
101	Icw(LDKx)	Permissible CW Current in LDKx (per channel)				500	mA
102	Vs(LDKx)	Saturation Voltage at LDKx	I(LDKx) = 450 mA, V(CIx) = V(CIx)@I(LDKx) = 500 mA			1.5	V
103	I0(LDKx)	Leakage Current in LDKx	ENx = lo, V(LDKx) = 12 V			100	µA
104	tr()	LDKx Current Rise Time Fast	Iop(LDKx) = 500 mA, I(LDKx): 10% → 90% Iop, V(ELVDS) = 0 V or VDD			1	ns
105	tf()	LDKx Current Fall Time Fast	Iop(LDKx) = 500 mA, I(LDKx): 90% → 10% Iop, V(ELVDS) = 0 V or VDD			1	ns
106	tr()	LDKx Current Rise Time Slow	Iop(LDKx) = 500 mA, I(LDKx): 10% → 90% Iop, V(ELVDS) = 30% VDD or 70% VDD, VDD = 5 V	5	10	40	ns
107	tf()	LDKx Current Fall Time Slow	Iop(LDKx) = 500 mA, I(LDKx): 90% → 10% Iop, V(ELVDS) = 30% VDD or 70% VDD, VDD = 5 V	5	10	40	ns
108	tr()	LDKx Current Rise Time Slow	Iop(LDKx) = 500 mA, I(LDKx): 10% → 90% Iop, V(ELVDS) = 30% VDD or 70% VDD, VDD = 3.3 V	10	30	90	ns
109	tf()	LDKx Current Fall Time Slow	Iop(LDKx) = 500 mA, I(LDKx): 90% → 10% Iop, V(ELVDS) = 30% VDD or 70% VDD, VDD = 3.3 V	10	30	90	ns
110	tp()	Propagation Delay Fast V(ENx) → I(LDKx)	V(ELVDS) = 0 V or VDD, Differential LVDS Rise and Fall Time < 0.5 ns	3	5	14	ns
111	CR()	Current Matching all Channels		0.9		1.1	
112	V(CIx)	Permissible Voltage at CIx		-0.3		VDD	V
113	Vt(CIx)	Threshold Voltage at CIx	I(LDKx) < 5 mA	0.5		1.2	V
114	V(CIx)	Operating Voltage at CIx	I(LDKx) = 500 mA, V(LDKx) > 1.8 V		2	2.9	V
115	Ipd(CIx)	Pull-Down Current at CIx	V(CIx) = 0.5. . . 5.5 V	1	2.5	5	µA
116	C(CIx)	Capacity at CIx	V(CIx) = 2 V	500	635	760	pF
117	Vc(LDKx)	Clamp Voltage at LDKx	I(LDKx) = 100 mA, tclamp < 1 ms, tclamp/T < 1:100	12.5		20	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0...5.5 V, AGND1...6 = GND, Tj = -25...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input EN1...6 (x = 1...6)							
201	Vt(TTL)hi	Input Threshold Voltage hi	V(ELVDS) < 35% VDD, TTL			2	V
202	Vt(TTL)lo	Input Threshold Voltage lo	V(ELVDS) < 35% VDD, TTL	0.8			V
203	Vhys(TTL)	Hysteresis	Vhys() = Vt()hi − Vt()lo; V(ELVDS) < 35% VDD, TTL	50			mV
204	I(ENx)	Pulldown Current	V(ELVDS) < 35% VDD, V() = 0.8 V... VDD, TTL	4	30	80	µA
205	R(ENx)	Differential Input Impedance at ENx	V(ELVDS) > 65% VDD, V(ENx) < VDD − 1.4 V, LVDS	14		28	kΩ
206	Vdiff	Differential Voltage	Vdiff = |V(EN1,3,5) − V(EN2,4,6)|; V(ELVDS) > 65% VDD, LVDS	200			mV
207	V()	Input Voltage Range	V(ELVDS) > 65% VDD, LVDS	0.6		VDD − 1.4	V
Input ELVDS							
301	V(ELVDS)	Voltage at ELVDS	ELVDS open	48	50	52	%VDD
302	Ri(ELVDS)			35	50	70	kΩ
303	Vt(ELVDS)	Threshold Voltage TTL Fast to TTL Slow		16	20	24	%VDD
304	Vt(ELVDS)	Threshold Voltage TTL Slow to Error		36	40	44	%VDD
305	Vt(ELVDS)	Threshold Voltage Error to LVDS Slow		56	60	64	%VDD
306	Vt(ELVDS)	Threshold Voltage LVDS Slow to LVDS Fast		74	80	84	%VDD
307	Vhys()	Hysteresis		10	25	50	mV
Ouput NER							
401	Vsat(NER)	Saturation Voltage at NER	ELVDS open, I(NER) = 2 mA			0.6	V
402	I(NER)	Current in NER	ELVDS open, V(NER) > 0.6 V	3	9	20	mA
Overtemperature							
501	Toff	Overtemperature Shutdown	rising temperature	130		170	°C
502	Ton	Overtemperature Release	falling temperature	120		160	°C
503	Thys	Hysteresis	Toff − Ton	5			°C
Power On							
601	VON	Power On Voltage VDD	rising voltage			2.9	V
602	VOFF	Power Down Voltage VDD	falling voltage	1.5			V
603	Vhys	Hysteresis		50		500	mV

CONFIGURATION INPUT ELVDS

Pin ELVDS selects between 6 channel TTL mode or 3 channel LVDS mode and chooses slow or fast switching speed. The unconnected pin ELVDS is an error condition signaled at pin NER with the laser current disabled.

Pin ELVDS connected to GND selects the six channel fast TTL mode. Pin ELVDS connected to 30% VDD selects the six channel slow TTL mode. Pin ELVDS connected to 70% VDD selects the three channel slow LVDS mode. Pin ELVDS connected to VDD selects the three channel fast LVDS mode.

An easy way to set the slow operation mode for TTL and LVDS mode is to connect a voltage divider at pin ELVDS. Figure 1 shows the recommended voltage divider for slow TTL mode and Figure 2 shows the recommended voltage divider for slow LVDS mode.

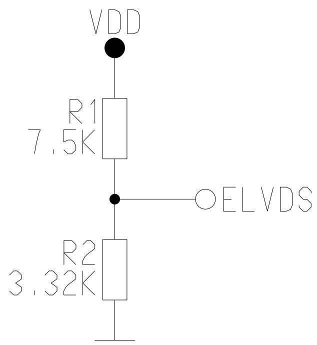


Figure 1: TTL Slow

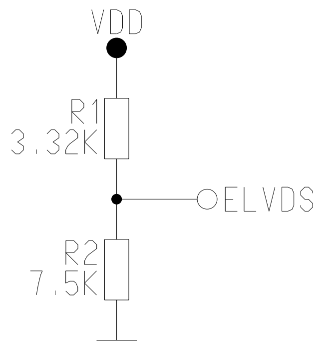


Figure 2: LVDS Slow

DIGITAL INPUTS EN1...6

EN1...6 are the digital switching inputs. With pin ELVDS set to *6 channel TTL mode*, each pin ENx enables the current sink at the respective LDKx. With pin ELVDS set to *3 channel LVDS mode*, the odd ENx pins are the positive and the even ENx pins are the negative LVDS inputs. EN1 and EN2 control LDK1 and LDK2, EN3 and EN4 control LDK3 and LDK4 and EN5 and EN6 control LDK5 and LDK6. For correct LVDS operation 100 Ω terminating resistors between the respective EPx and ENx pins, very close to the inputs, are strongly recommended. Input pins from unused channels have to be connected to GND (TTL operation) resp. EPx to GND and ENx to VDD (LVDS operation).

ANALOG CURRENT CONTROL VOLTAGE INPUTS CI1...6

The Voltage at pins CI1...6 set the current value at pins LDK1...6. The figures 3 and 4 shows the temperature dependency of the current at LDK versus the Voltage at CI. The figures 5 and 6 shows the min., typ. and max. variations between devices.

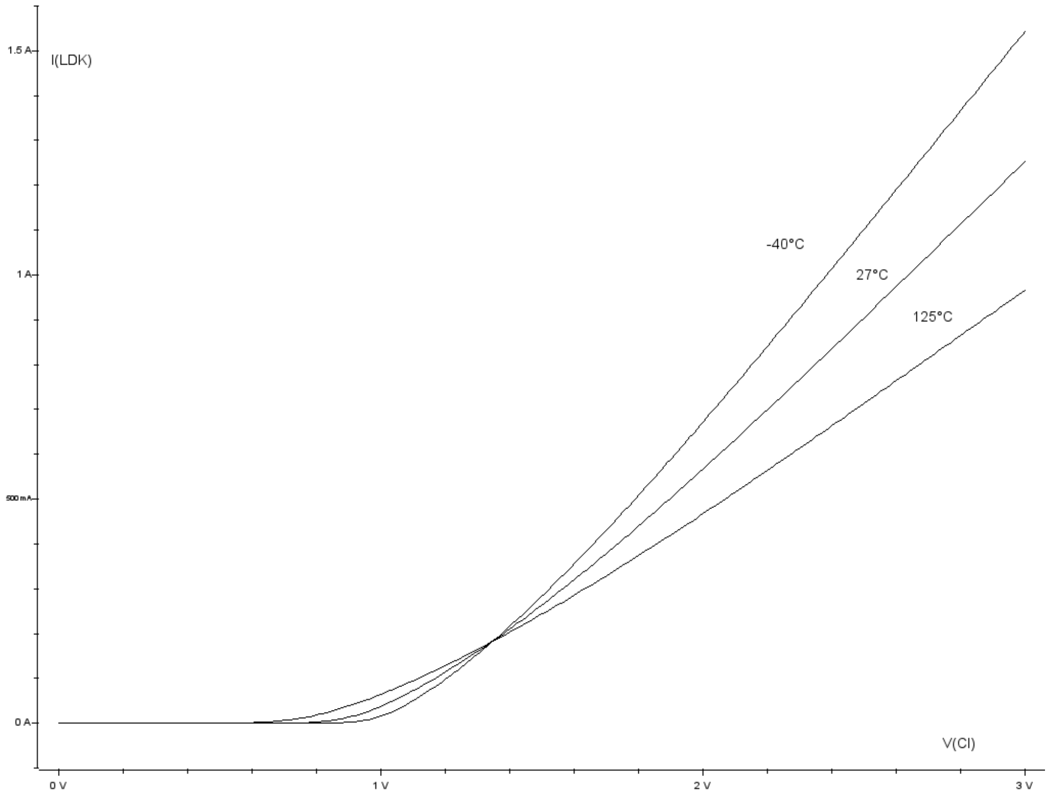


Figure 3: I(LDK) vs. V(CI) at VDD = 5 V

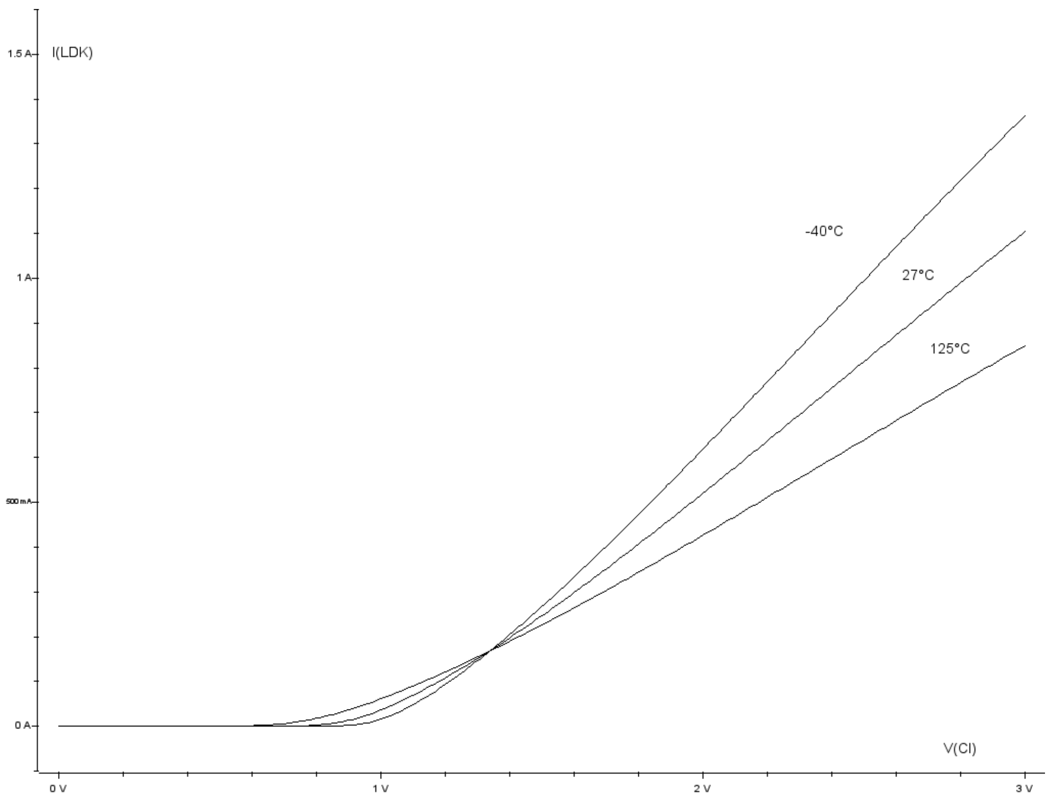


Figure 4: I(LDK) vs. V(CI) at VDD = 3.3 V

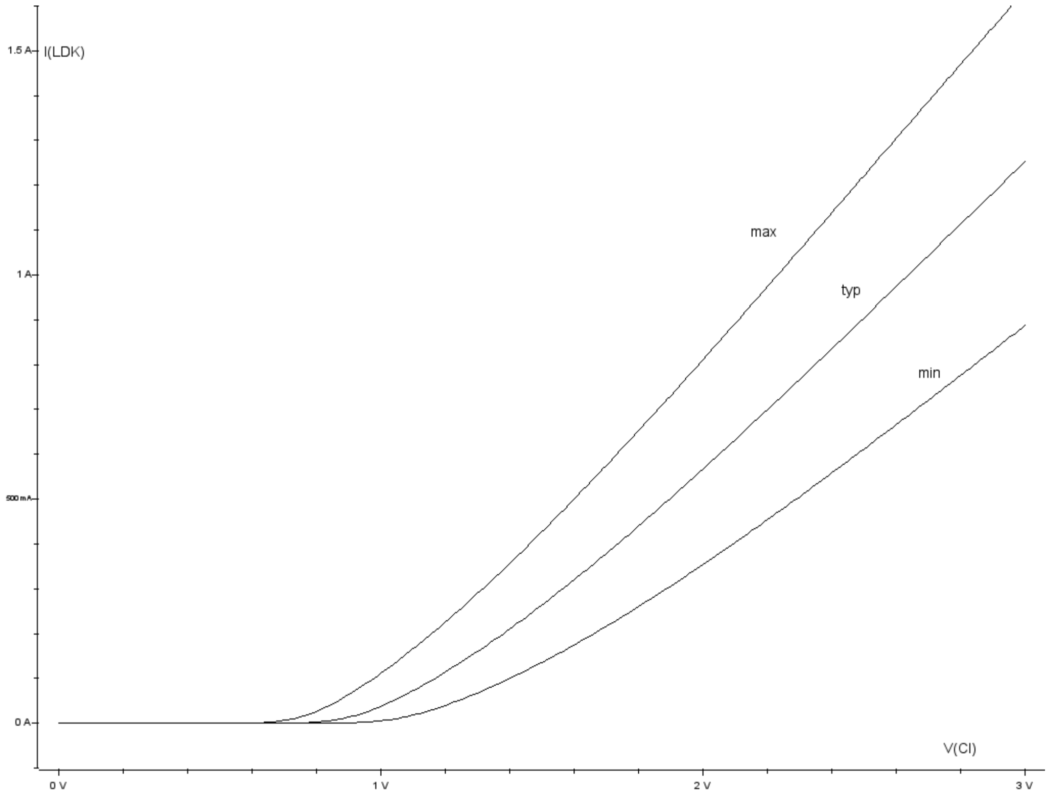


Figure 5: I(LDK) vs. V(CI) at VDD = 5 V and TJ = 27 °C

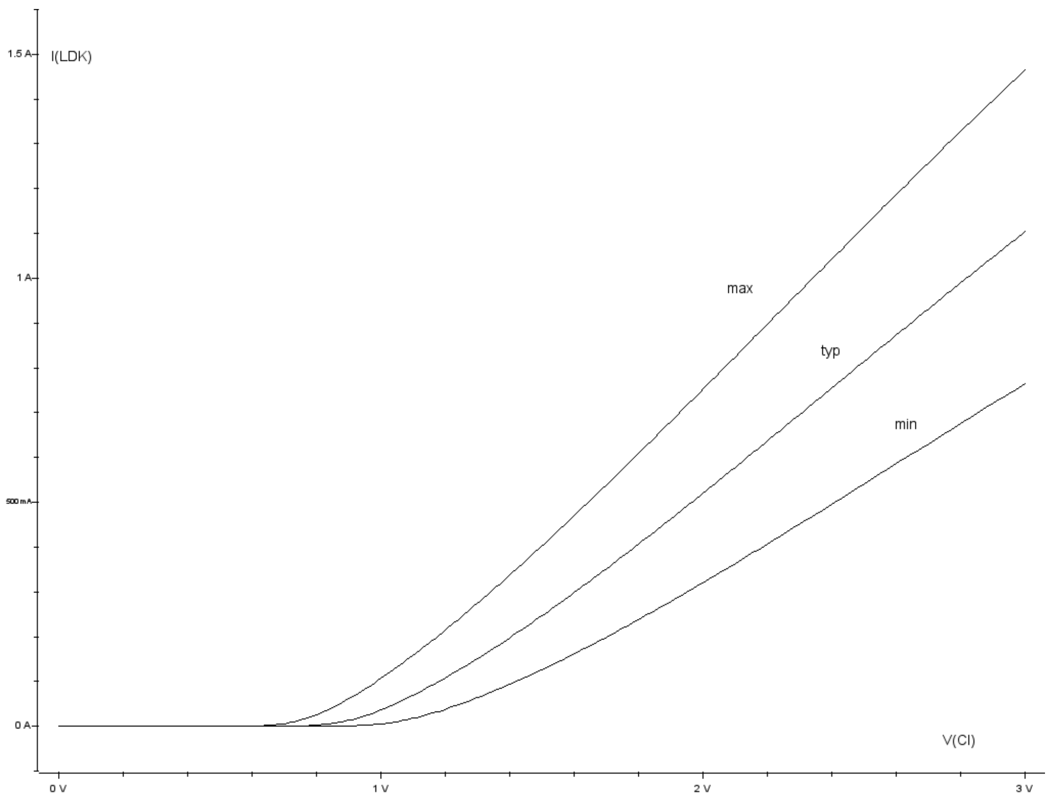


Figure 6: I(LDK) vs. V(CI) at VDD = 3.3 V and TJ = 27 °C

LASER OUTPUTS LDK1...6

LDK1...6 are the current pins for the laser diode cathode. For high speed operation connect the laser diode as close as possible to this pins to minimize the inductance. It may still be necessary though to use an RC snubber network for damping LC oscillations.

ANALOG GROUNDS AGND1...6

AGND1...6 are the ground pins for the channels. It is recommended to connect all AGND1...6 pins to GND.

ERROR OUTPUT NER

The open drain NER pin is a low-active error output. Signalled errors are ELVDS open or at 50% VDD, VDD undervoltage and thermal shutdown.

THERMAL SHUTDOWN

iC-HG is protected by an integrated thermal shutdown feature. When the shutdown temperature is reached all channels are disabled. Falling temperature after this shutdown will unconditionally enable all channels again. Necessary precaution to prevent damage of the laser may be to also disable any external control circuits for the laser output power power or current control during thermal shutdown. The error signal at pin NER can be used to e.g. disable the control circuit.

APPLICATION EXAMPLES

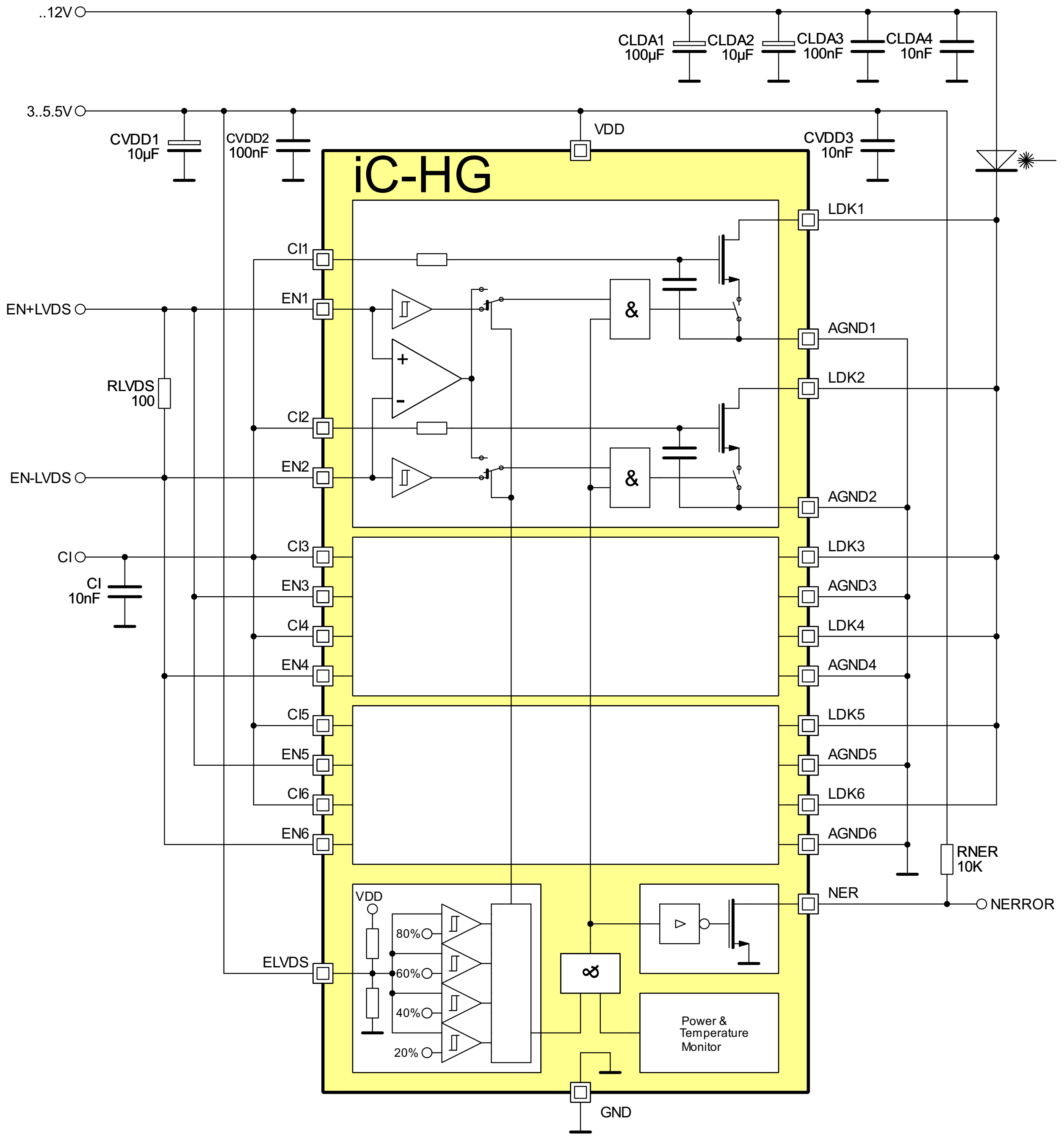


Figure 7: 1 channel LVDS fast

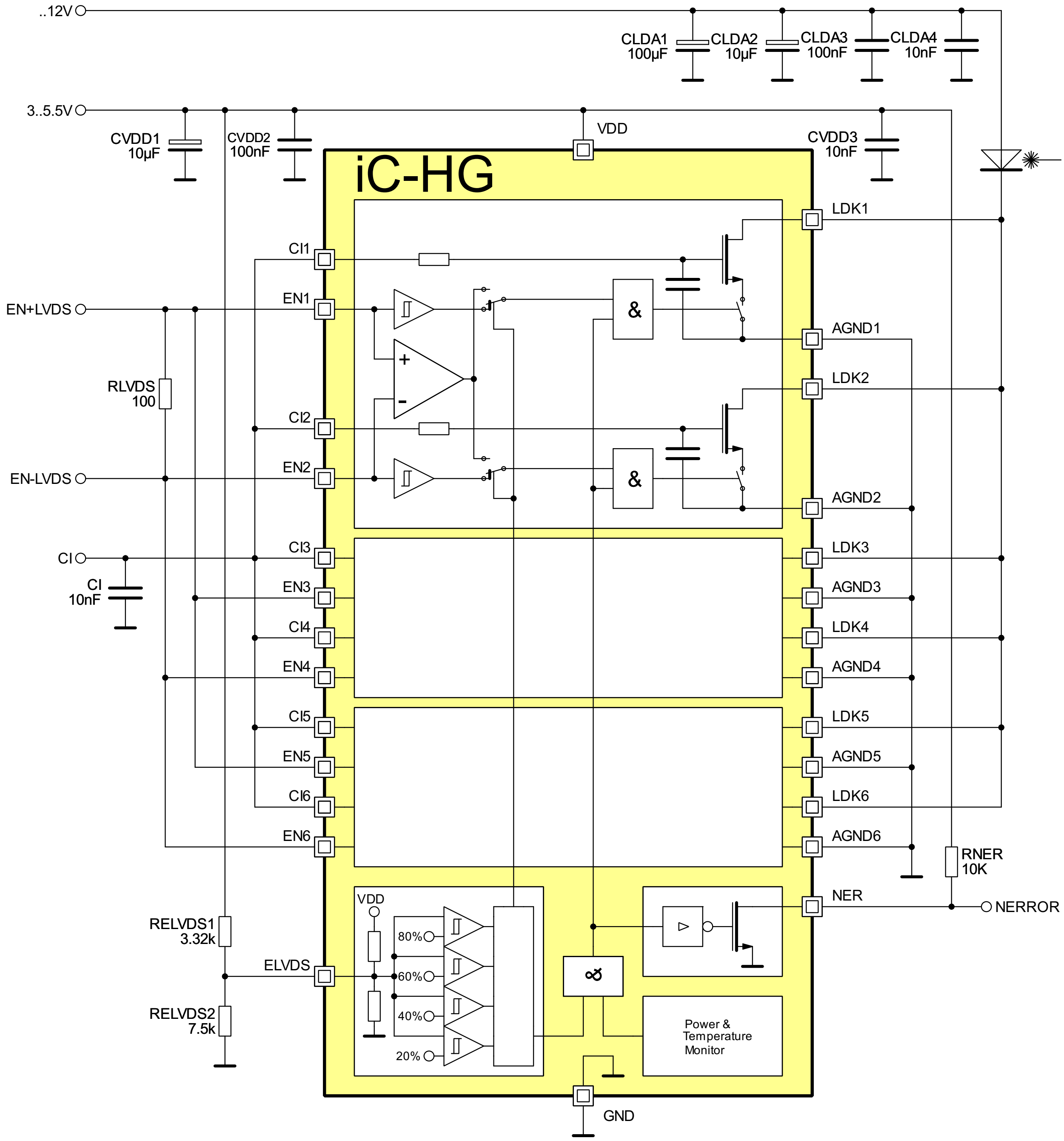


Figure 8: 1 channel LVDS slow

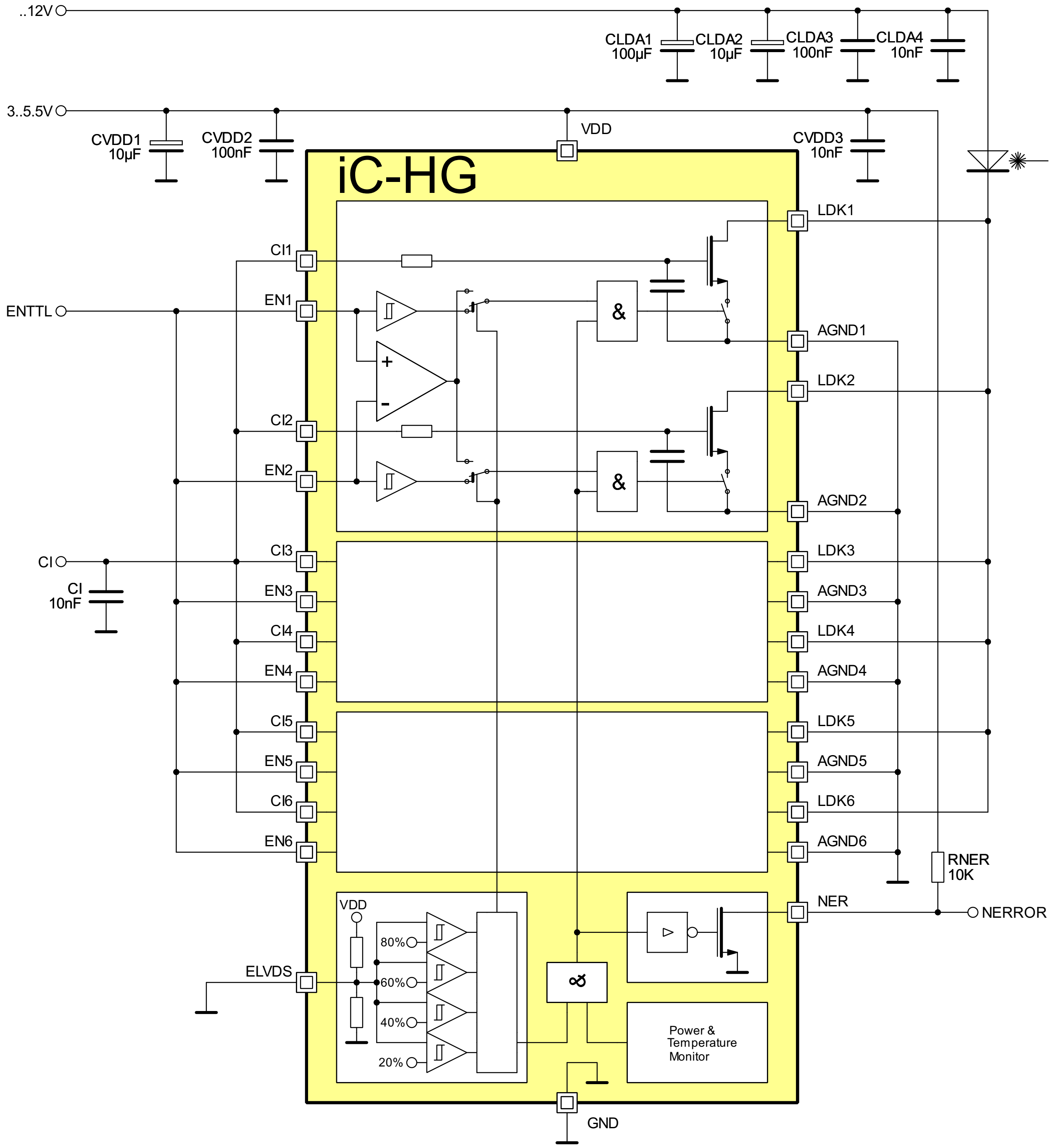


Figure 9: 1 channel TTL fast

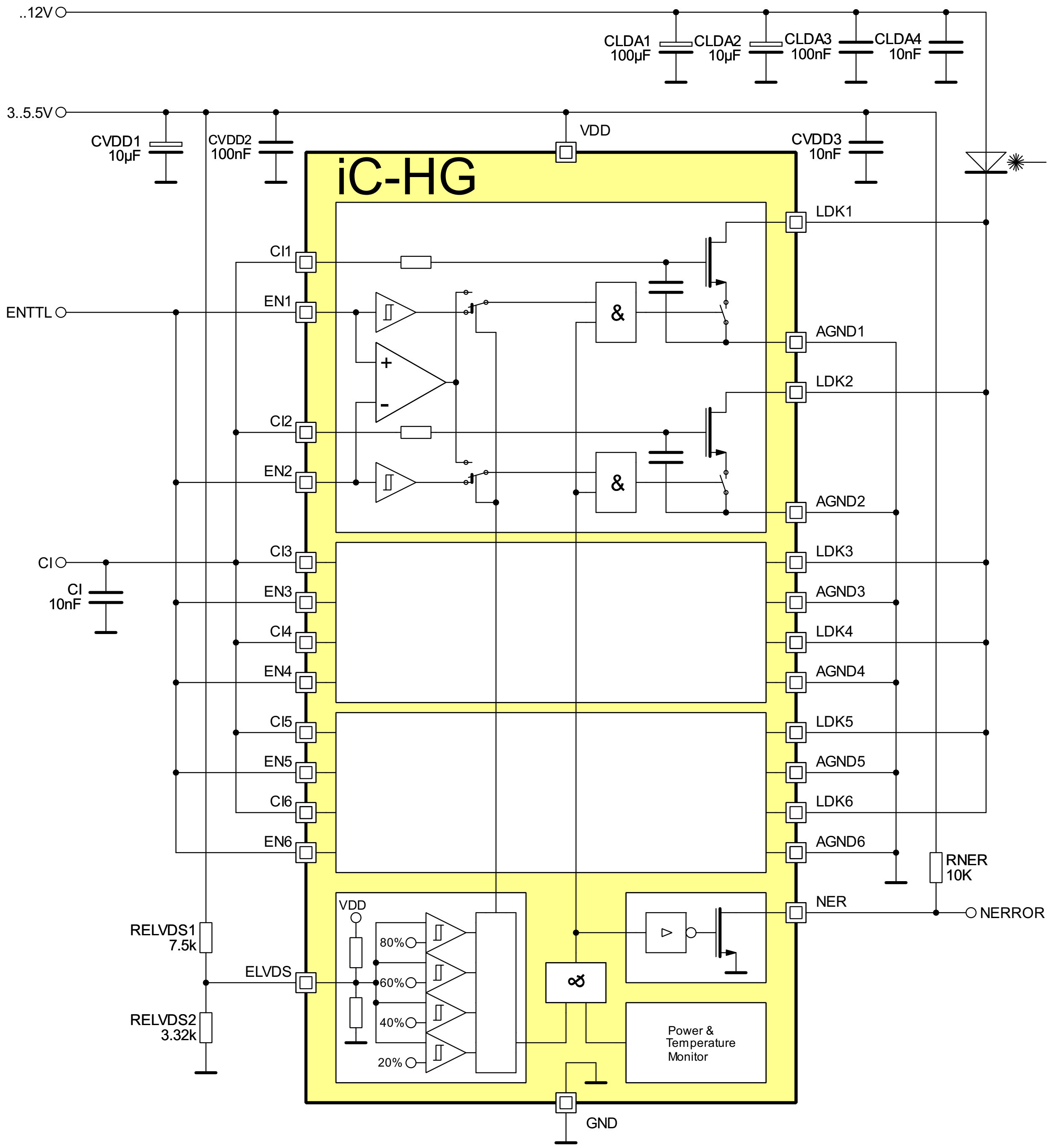


Figure 10: 1 channel TTL slow

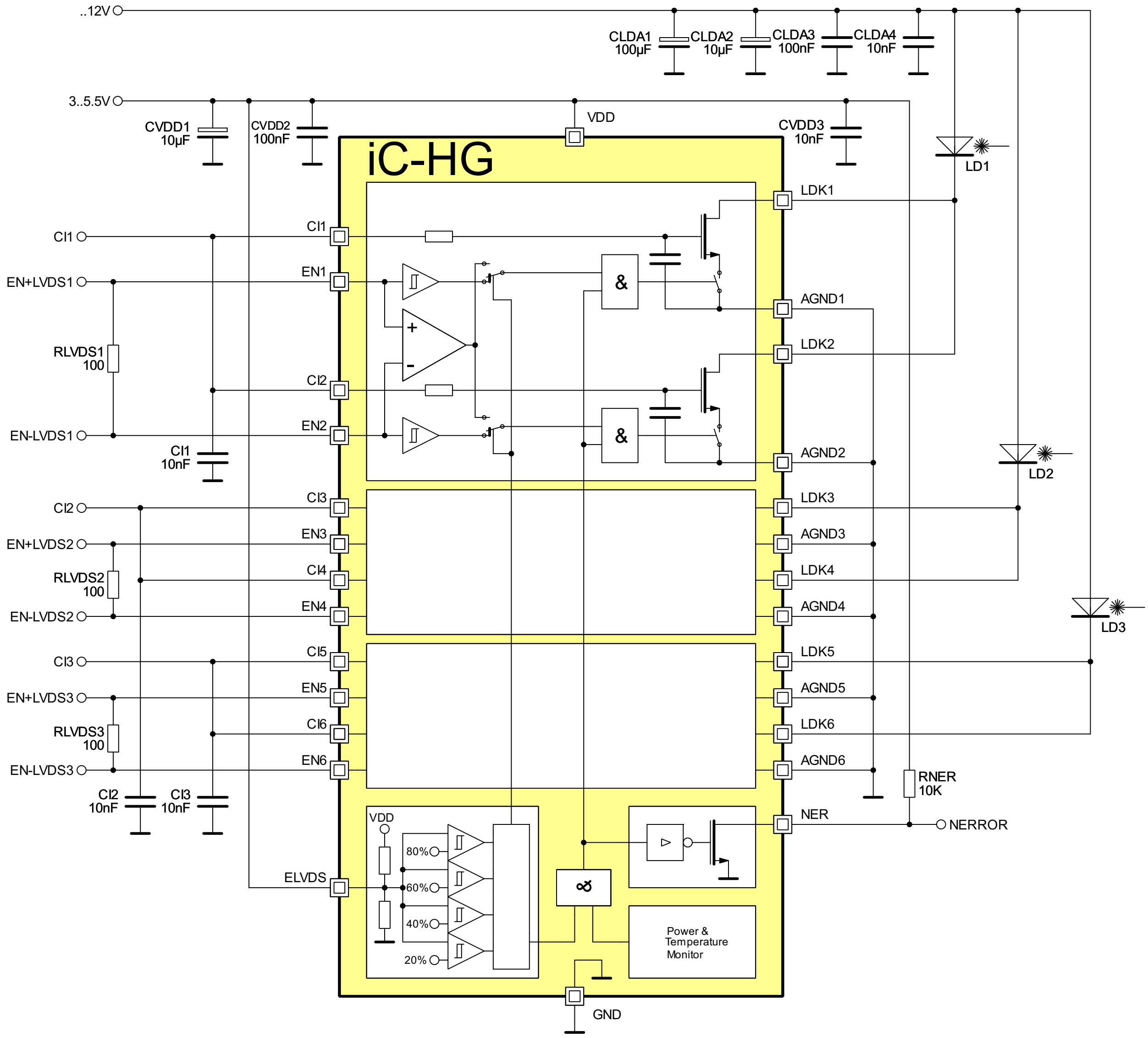


Figure 11: 3 channel LVDS fast

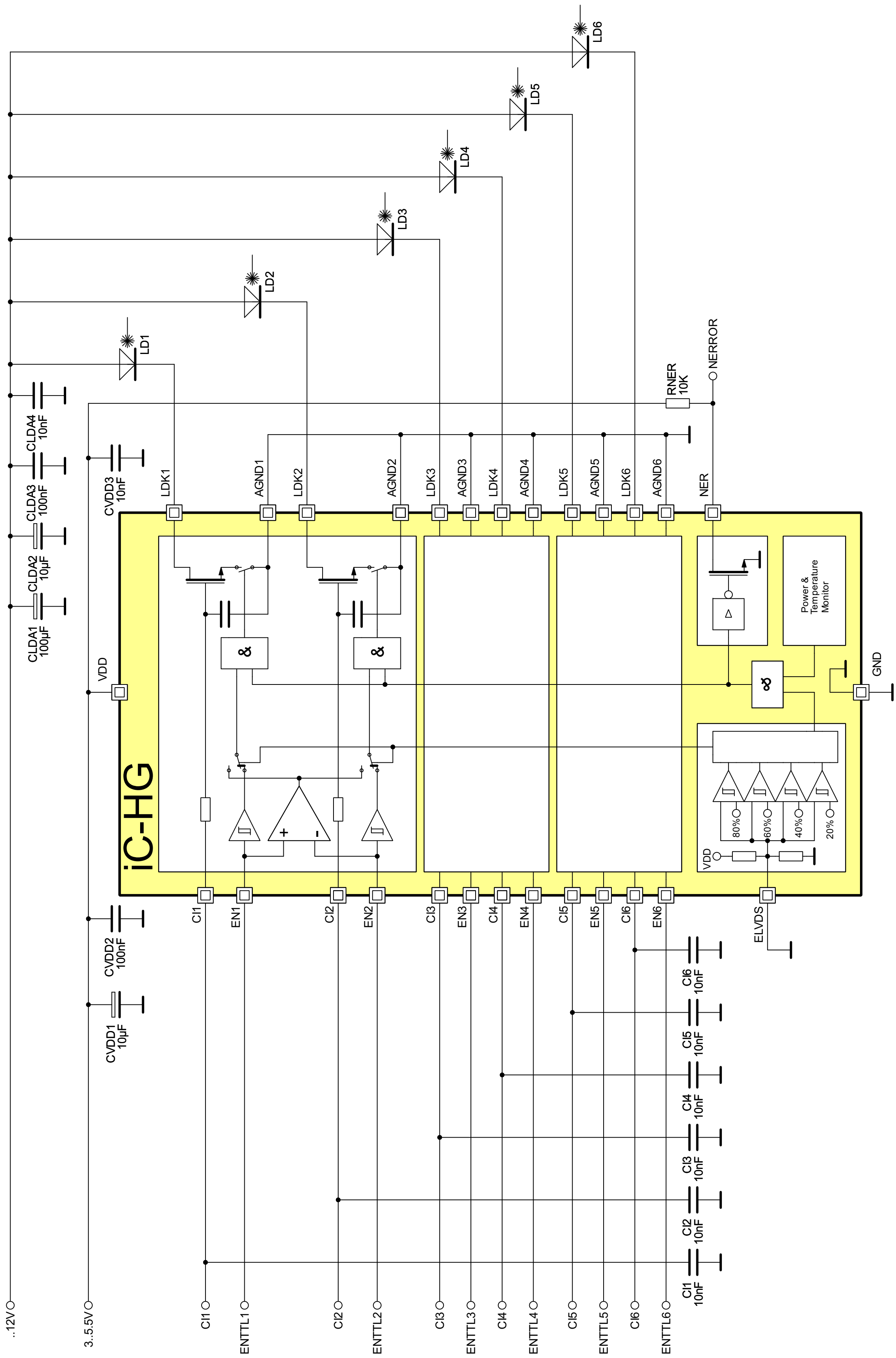


Figure 12: 6 channel TTL fast

EVALUATION BOARD

iC-HG comes with an evaluation board for test purpose. Figures 13 and 14 show both the schematic and the component side of the evaluation board.

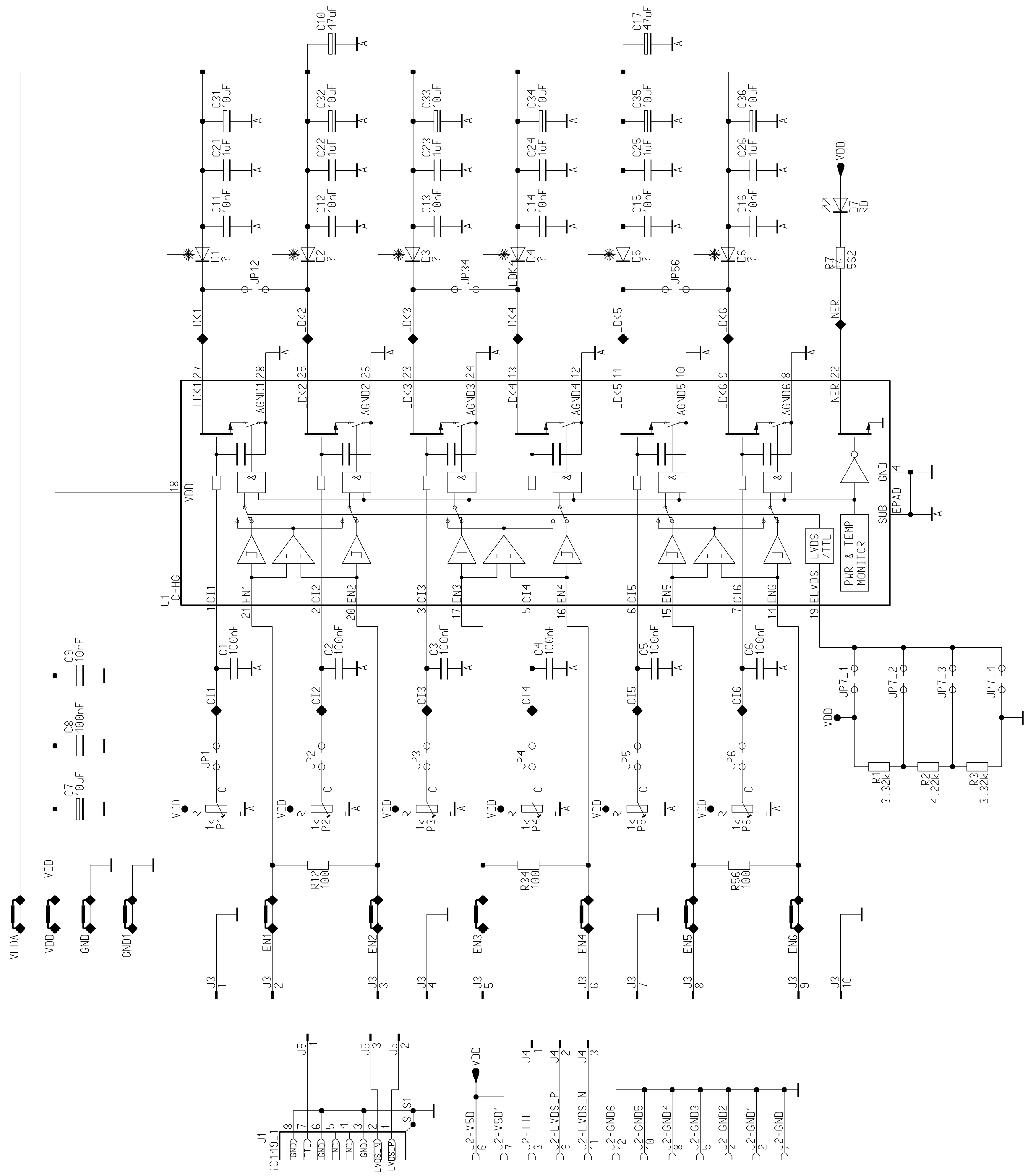


Figure 13: Schematic of the evaluation board

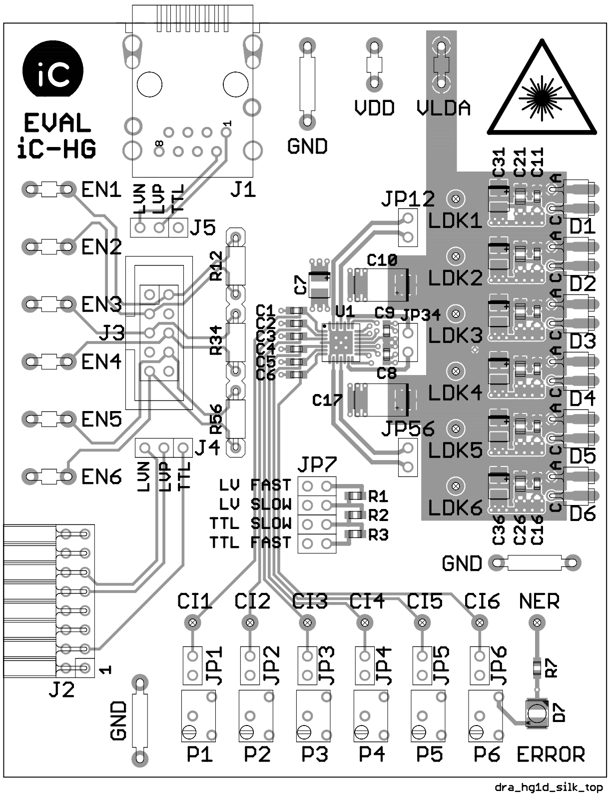


Figure 14: Evaluation board (component side)

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We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

ORDERING INFORMATION

Type	Package	Order Designation
iC-HG	QFN28 5 mm x 5 mm Evaluation Board	iC-HG QFN28 iC-HG EVAL HG1D

For technical support, information about prices and terms of delivery please contact:

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